

Appl. No. 09/805,535
Amdt. Dated 09-01-2005
Reply to Office action of 06-01-2005

REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the Office Action mailed June 1, 2005. In the Office Action, the Examiner rejected claims 1-30 under 35 U.S.C. §102(b). Applicants have amended claim 1 to correct minor informalities. Applicants submit that the newly-added claims introduce no new matter. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Claim Objections

1. The Examiner objects to claim 1 due to minor informalities. The Examiner indicated that the term "the PN clock signal" lacks antecedent bases and should be changed to "a PN clock signal". Applicants have amended claim 1 to correct the informalities.

Applicant respectfully requests that the Examiner withdraw the objection to claim 1.

Rejection Under 35 U.S.C. § 102

1. In the Office Action, the Examiner rejected claims 1-30 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,901,171 issued to Kohli et al. ("Kohli"). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of anticipation.

Kohli discloses a triple multiplexing spread spectrum receiver. A channel coder block 112 includes a coder NCO 136 and a code generator 138. The coder NCO 136 creates a Gen_Enable whenever a Phase Accumulator 148 overflows (Kohli, col. 19, lines 12-16). A configuration using 11-bit registers is used so that each register is used 186 times per msec to process all 1023 bits of a C/A code repetition (Kohli, col. 22, lines 7-10)..

Kohli does not disclose, either expressly or inherently, among other things, (1) a control circuit to generate a channel enable signal, (2) the channel enable signal selecting a channel for a satellite in a GPS, (3) the channel operating at a C/A clock signal, (4) an increment register to store an increment value for the selected channel, and (5) an accumulator to generate a PN clock signal using the increment value.

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To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergasa Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989). Since the Examiner failed to show that Kohli teaches or discloses any one of the above elements, the rejection under 35 U.S.C. §102 is improper.

Kohli merely discloses a Gen_Enable signal being applied to the Code Generator 138 to cause a new code to be generated (Kohli, col. 19, lines 49-50). Therefore, the Gen_Enable signal is not the channel enable signal because it does not select a channel for a satellite in a GPS. The Coder Block 112 is caused to sequence through as many sets of 240 different code delays as necessary to acquire the satellite signals from a particular space vehicle (Kohli, col. 17, lines 26-29). It is not a control circuit because it does not generate a channel enable signal to select a channel for a satellite.

Furthermore, the Examiner failed to identify elements in Kohli that correspond to several elements in the rejected claims, including an increment register and the accumulator.

Regarding claim 2, 12, and 22, the Examiner failed to identify teachings of Kohli related to the control information including at least one of channel select information, an initial count, the increment value, and PN command.

Regarding claims 3, 12, and 23, the Examiner failed to identify teachings of Kohli related to the control circuit comprising a decoder, a channel enable register, a counter, and a logic circuit.

Regarding claims 4, 14, and 24, the Examiner states that Figure 6 discloses an accumulating register and an adder coupled to the register for storing an output of the NCO. However, these registers including the Doppler multiplier 132, four 4-bit registers, two adders, another pair of 5-bit registers and a quantizer are used to form the dopIOut and dopQOut (Kohli, col.18, lines 56-59). They are not used to provide the PN clock, or a sum of the increment value and the NCO value using a shift command.

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Regarding claims 5-8, 15-18, and 25-28, the Examiner states that the code generator 138 produces the next bit for the C/A code and this bit is applied serially to code shift register 170. However, the next bit for the C/A code is not the increment value. Furthermore, Kohli does not disclose using a shift command from a PN command.

Regarding claims 10, 20, and 30, the Examiner failed to identify teachings of Kohli related to the channel enable signal selecting a channel for a satellite and being one of the twelve satellites in the GPS.

The Examiner should set forth in the Office Action the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate. See MPEP 706.02(j). The goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of a patentability and otherwise reply completely at the earliest opportunity. See MPEP 706.

Therefore, Applicants believe that independent claims 1,11, and 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejection under 35 U.S.C. §102(b) be withdrawn.

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Conclusion

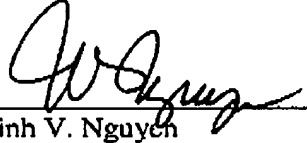
Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 1, 2005

By


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